CLAIMS

What is claimed is:

1. A substrate on which to mount an integrated circuit (IC) having a first dense formation of lands, the substrate comprising:

a second dense formation of lands on a surface thereof formed in a geometrical pattern to maximize the density of the second dense formation of lands, while constrained by the size of individual lands and by the width and spacing of substrate traces coupled to the lands.

2. The substrate recited in claim 1, wherein the density of the second dense formation of lands equals the reciprocal of (Tw + Ts), wherein Tw equals the width of the substrate traces and Ts equals the spacing between the substrate traces.

3. The substrate recited in claim 1, wherein the second dense formation of lands is formed as a plurality of zigzag rows.

4. The substrate recited in claim 3, wherein the plurality of zigzag rows are substantially parallel.

5. The substrate recited in claim 1, wherein the second dense formation of lands is formed in a pattern from the group consisting of a zigzag pattern, a wave pattern, an undulating pattern, a vertical stack pattern, and any combination of such patterns.

6. The substrate recited in claim 1, wherein the second dense formation of lands is formed in a pattern comprising a combination of a face center rectangular pattern and a pattern from the group consisting of a zigzag pattern, a wave pattern,

an undulating pattern, a vertical stack pattern, and any combination of a zigzag pattern, a wave pattern, an undulating pattern, and a vertical stack pattern.

7. An electronic package comprising:

an integrated circuit (IC) comprising a first plurality of lands on a surface thereof, including a first dense formation of lands;

a substrate comprising a second plurality of lands on a surface thereof, including a second dense formation of lands formed in a geometrical pattern to maximize the density of the second dense formation of lands, while constrained by the size of the second dense formation of lands and by the width and spacing of substrate traces coupled to the second dense formation of lands; and

elements coupling the first plurality of lands to the second plurality of lands.

8. The electronic package recited in claim 7, wherein the density of the second dense formation of lands equals the reciprocal of (Tw + Ts), wherein Tw equals the width of the substrate traces and Ts equals the spacing between the substrate traces.

9. The electronic package recited in claim 7, wherein the second dense formation of lands is formed as a plurality of zigzag rows at the periphery of the surface of the substrate.

10. The electronic package recited in claim 7, wherein the second dense formation of lands is formed in a pattern from the group consisting of a zigzag pattern, a wave pattern, an undulating pattern, a vertical stack pattern, and any combination of such patterns.

11. The electronic package recited in claim 7, wherein the IC is an unpackaged die.

12. The electronic package recited in claim 7, wherein the IC is a packaged die.

13. An electronic system comprising least one electronic package comprising:

an integrated circuit (IC) comprising a first plurality of lands on a surface thereof, including a first dense formation of lands;

a substrate comprising a second plurality of lands on a surface thereof, including a second dense formation of lands formed in a geometrical pattern to maximize the density of the second dense formation of lands, while constrained by the size of the second dense formation of lands and by the width and spacing of substrate traces coupled to the lands; and

elements coupling the first plurality of lands to the second plurality of lands.

14. The electronic system recited in claim 13, wherein the second dense formation of lands is formed in a pattern from the group consisting of a zigzag pattern, a wave pattern, an undulating pattern, a vertical stack pattern, and any combination of such patterns.

15. The electronic system recited in claim 13, wherein the IC is an unpackaged die.

16. A data processing system comprising:

a bus coupling components in the data processing system;

a display coupled to the bus;

external memory coupled to the bus; and

a processor coupled to the bus and including at least one electronic package comprising:

an integrated circuit (IC) comprising a first plurality of lands on a surface thereof, including a first dense formation of lands;

a substrate comprising a second plurality of lands on a surface thereof, including a second dense formation of lands formed in a geometrical pattern to maximize the density of the second dense formation of lands, while constrained by

the size of the second dense formation of lands and by the width and spacing of substrate traces coupled to the lands; and

elements coupling the first plurality of lands to the second plurality of lands.

17. The data processing system recited in claim 16, wherein the second dense formation of lands is formed in a pattern from the group consisting of a zigzag pattern, a wave pattern, an undulating pattern, a vertical stack pattern, and any combination of such patterns.

18. The data processing system recited in claim 16, wherein the IC is an unpackaged die.

19. A method comprising:

forming on a substrate surface a plurality of traces, the traces having at least a predetermined width and a predetermined spacing from one another; and

forming on the substrate surface a plurality of lands, each coupled to a corresponding one of the plurality of traces, and each having at least a predetermined size, the plurality of lands being formed in a geometrical pattern that maximizes the density of such lands while constrained by the land size and by the width and spacing of the traces.

20. The method recited in claim 19, wherein the density of the plurality of lands equals the reciprocal of (Tw + Ts), wherein Tw equals the width of the traces and Ts equals the spacing between the traces.

21. The method recited in claim 19, wherein the plurality of lands are formed as a plurality of zigzag rows.

22. The method recited in claim 21, wherein the plurality of zigzag rows are substantially parallel.

23. The method recited in claim 19, wherein the plurality of lands are formed in a pattern from the group consisting of a zigzag pattern, a wave pattern, an undulating pattern, a vertical stack pattern, and any combination of such patterns.

24. The method recited in claim 19, wherein the plurality of lands are formed in a pattern comprising a combination of a face center rectangular pattern and a pattern from the group consisting of a zigzag pattern, a wave pattern, an undulating pattern, a vertical stack pattern, and any combination of a zigzag pattern, a wave pattern, an undulating pattern, and a vertical stack pattern.

25. A method of forming a substrate comprising a plurality of layers, the method comprising:

for a first layer, forming a first plurality of traces having at least a predetermined width and a predetermined spacing from one another;

for a second layer, forming a second plurality of traces having at least a predetermined width and a predetermined spacing from one another;

for the first and second layers, forming a plurality of vias to couple ones of the first plurality of traces to ones of the second plurality of traces; and

for the second layer, forming a first plurality of lands each coupled to a corresponding one of the plurality of traces of the second layer, and each having at least a predetermined size, the first plurality of lands being formed in a geometrical pattern that maximizes the density of the first plurality of lands while constrained by the land size and by the width and spacing of the traces of the second layer.

26. The method recited in claim 25, wherein each via has at least a predetermined size, the method further comprising:

for the second layer, forming a second plurality of lands, each coupled through a corresponding via to a corresponding one of the plurality of traces of the first layer, the second plurality of lands being formed in a geometrical pattern that

maximizes the density of the second plurality of lands while constrained by the width and spacing of the traces of the first layer.

27. The method recited in claim 26, wherein the second plurality of lands is formed in a geometrical pattern that maximizes the density of the second plurality of lands while additionally constrained by the via size.

28. The method recited in claim 25, wherein the density of the first plurality of lands equals the reciprocal of (Tw + Ts), wherein Tw equals the width of the traces of the second layer and Ts equals the spacing between the traces of the second layer.

29. The method recited in claim 25, wherein the first plurality of lands are formed as a plurality of zigzag rows.

30. The method recited in claim 29, wherein the plurality of zigzag rows are substantially parallel.

31. The method recited in claim 25, wherein the first plurality of lands are formed in a pattern from the group consisting of a zigzag pattern, a wave pattern, an undulating pattern, a vertical stack pattern, and any combination of such patterns.

32. A method comprising:

forming lands on a substrate surface in a geometrical pattern to maximize the density of such lands while constrained by the land size and by the width and spacing of traces coupled to the lands and formed on the substrate surface; and

coupling lands on an integrated circuit (IC) to corresponding lands on the substrate surface.

33. The method recited in claim 32, wherein the density of the plurality of lands equals the reciprocal of (Tw + Ts), wherein Tw equals the width of the traces and Ts equals the spacing between the traces.

34. The method recited in claim 32, wherein the IC is an unpackaged die.

35. The method recited in claim 32, wherein the IC is a packaged die.